

First Named Inventor	Frankie F. Roohparvar
Serial No.	09/943,399
Filing Date	August 30, 2001
Group Art Unit	2818
Examiner Name	Ly D. Pham
Attorney Docket No.	400.130US01

RESPONSE TO
NON-FINAL OFFICE
ACTION

Title: FLASH MEMORY WITH RDRAM INTERFACE

Commissioner for Patents
Washington, D.C. 20231

In response to the non-final Office Action mailed on December 19, 2002, please consider the following remarks:

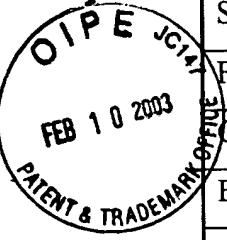
REMARKS

Rejections Under U.S.C. § 103

Claims 1 – 4, 14 – 15, and 18 were rejected under 35 U.S.C. § 103(a) as being anticipated by *Chen et al.* (U.S. Patent No. 6,324,602). Claims 16, 17, and 19 were rejected under 35 U.S.C. § 103(a) as being anticipated by *Chen et al.* in view of *Deneroff et al.* (U.S. Patent No. 6,215,686). The Applicants respectfully traverse these rejections.

Chen et al. discloses an input/output interface for an integrated circuit device. *Chen et al.* additionally discloses a Rambus memory device as applied to a DRAM (column 1, line 66 – col. 2, line 9), a flash memory device, and a DRAM that transfers data on both edges of a clock (column 1, lines 55 – 57). However, *Chen et al.* neither teaches nor suggests a flash memory that has Rambus-compatible interconnections and circuitry to provide input and output data on rising and falling edges of a clock as claimed in the present application. The flash memory device mentioned in *Chen et al.* is mentioned only in reference to typical memory devices and no detail is provided as to any flash memory functionality.

The DRAM disclosed in *Chen et al.* cannot be equated with a flash memory since they have different bus interconnections, functions, and uses. The flash memory of the present invention provides a Rambus-compatible non-volatile memory device that uses the same bus as a Rambus device while transferring data on both edges of a clock signal.



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Deneroff et al. discloses a memory system that has switches for controlling data transfer. *Deneroff et al.* neither teaches nor suggests Applicants' invention for a flash memory as claimed in the present application. Therefore, even if it were obvious to combine *Chen et al.* with *Deneroff et al.*, the combination does not disclose Applicants' invention.

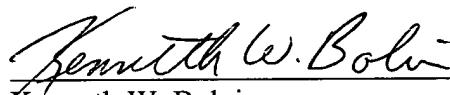
CONCLUSION

In view of the above remarks, Applicant respectfully submits that the claims are in condition for allowance and requests reconsideration of the application and allowance of the claims.

The Examiner is invited to contact Applicants' representatives at direct dial (612) 312-2211 if there are any questions regarding this Response or if prosecution of the present application may be assisted thereby. No new matter has been added and no additional fee is required by this response.

Respectfully submitted,

Date: 2/5/03



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TRANSMITTAL
FORM UNDER
37 CFR 1.8

(LARGE ENTITY)

Title: FLASH MEMORY WITH RDRAM INTERFACE

Commissioner for Patents
Washington, D.C. 20231

The following documents are enclosed:

A Response to Office Action (2 pgs.); and
 A return postcard.

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Fee Calculation							
	Number of Claims		Prv. Amt.	Extra Claims		Fee	
Total Claims		-20			X	\$18	= \$.00
Independent Claims		-3			X	\$84	= \$.00
							=
							Total \$.00

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Signature	<i>Kenneth W. Bolvin</i>			Date	<i>2/5/03</i>

Certificate of Mailing

I certify that this correspondence and the identified documents are being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D. C. 20231 on February 5, 2003.

Name	Signature
Rhonda L. Hutar	<i>Rhonda L. Hutar</i>

(LARGE ENTITY TRANSMITTAL UNDER 37 C.F.R. 1.8)